SV615XP Series Datasheet

Low Power WiFi single Band 802.11 b/g/n SoC with USB/SDIO/SPI interface.

General Description

The SV615XP is a low-power single chip device with the highest level of integration for internet of thing embedded systems. It is designed to support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~MCS7, HT20/HT40, 800ns and 400ns guard interval.

It includes a single band WLAN CMOS efficient power amplifier (PA) and an internal low noise amplifier (LNA). The Radio Frequency Front-end is single-ended bi-directional input and output.

The SV615XP has additional LDOs and DCDC buck convertor that could provide noise isolation for digital and analog supplies and excellent power efficient with minimum BOM cost.

While they both provide multiple peripheral interfaces including UART_DEBUG, etc.

SV615XP series include:

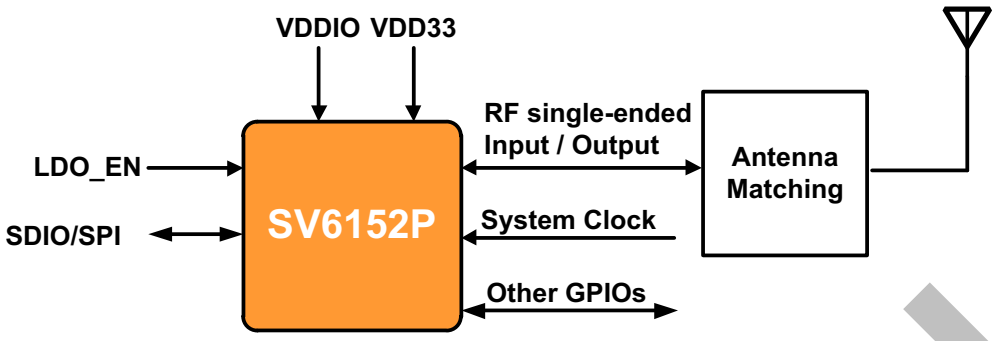
SV6155P (USB interface)

SV6152P (SDIO/SPI interface)

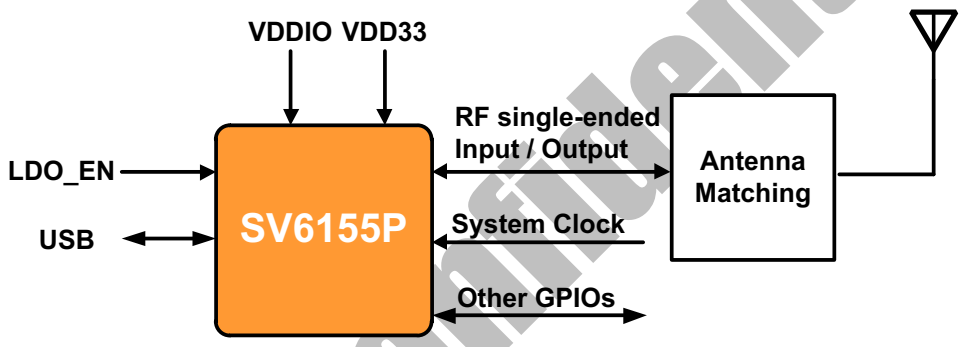
The only external clock source needed for SV615XP based designs is a high speed crystal or oscillator. SV6155P only support two reference clocks which are 25MHz and 40MHz. SV6152P support a variety of reference clocks which include 19.2, 20, 24, 25, 26, 38.4, 40 and 52 MHz.

SV615XP Features

- All CMOS IEEE 802.11 b/g/n single chip
- Single stream 802.11n provides highest throughput and superior RF performance for embedded system
- Advanced 1x1 802.11n features:
  - Full / Half Guard Interval
  - Frame Aggregation
  - Space Time Block Coding (STBC)
  - Greenfield mode
- Integrated WLAN CMOS efficient power amplifier with internal power detector and closed loop power calibration
- Package
  - QFN 48L, 6x6 mm, 0.4mm pitch



SV6152P System Block Diagram



SV6155P System Block Diagram

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Revision History

Version	Date	Description
1.0	2019/12/30	Initial release
1.1	2020/06/10	• Updated Figure 1: SV615XP Block Diagram • Updated chapter 1.4 SYSTEM/chapter • Updated chapter 1.5 HOST INTERFACE • Updated Figure 2: SV615XP Power Connection • Updated Figure 4 : Power-on sequence • Added Figure 5 : Reset Timing • Added Table 2 : Reset Timing Parameters • Added SPI Timing Waveform, Figure 6/Table 3 • Updated the Operating Temperature from -20°C to -40°C, Table 9/Table 26 • Updated DC Characteristics, Table 8/Table 13 • Update Pin Descriptions, chapter 8/Figure 10/Table 19 • Updated strapping table, Table 20/Table 21/Table 22/Table 23/Table 24 • Updated Table 25: The PAD multiplex for each PAD • Deleted UVLO feature • Deleted 1.8V power from DVDDIO1/DVDDIO3

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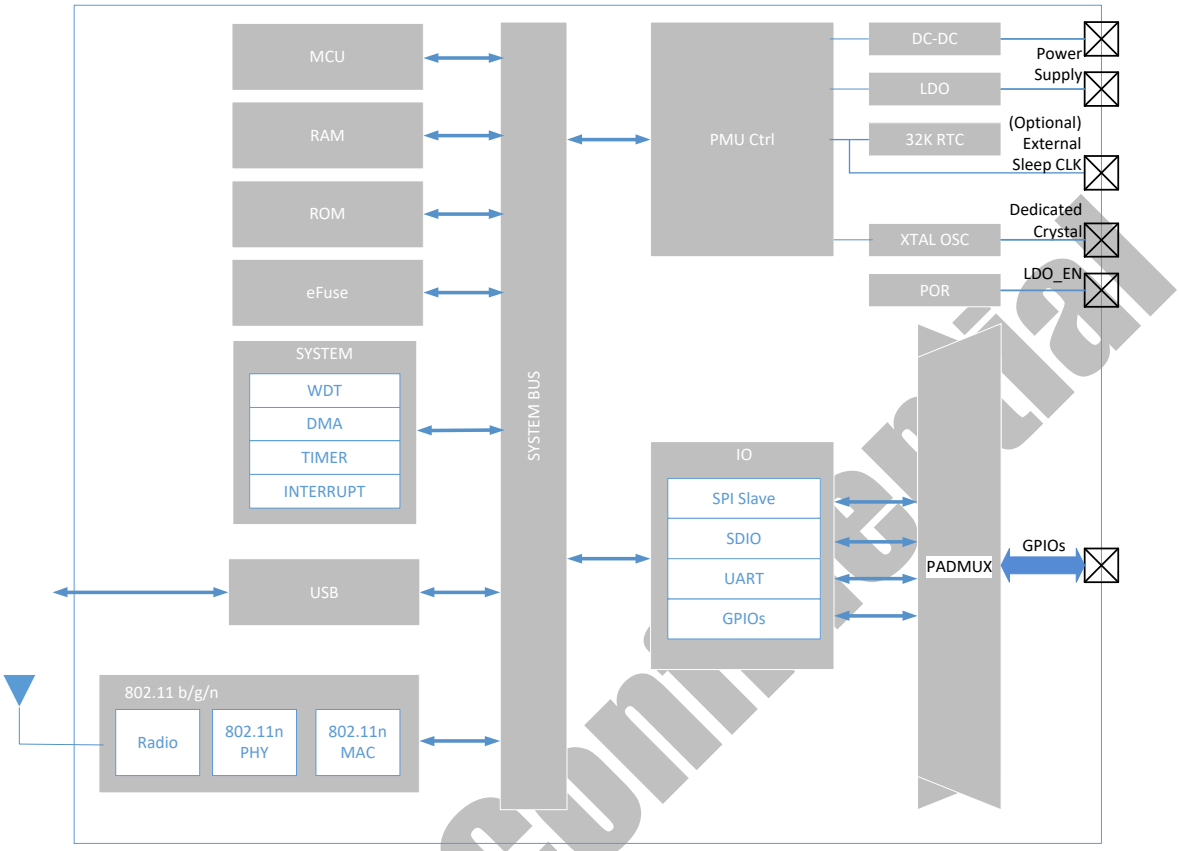


Figure 1: SV615XP Block Diagram

1.1 General Description

The SV615XP WLAN is designed to support IEEE 802.11 b/g/n single stream with the state of-the-art design techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The SV615XP WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and achieve extreme low power consumption at sleep state to extend the battery life. The SV615XP WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.

1.2 MAC FEATURES

- 802.11 b/g/n/e/i/d
- 802.11n features
  - A-MPDU Tx & Rx
  - Support immediate Block-Ack
- AP/STA mode
  - Soft-AP
- Rate adaption mechanism
- WFA features
  - WEP/TKIP/WPA/WPA2
  - WMM/WMM PS

1.3 PHY FEATURES

- 802.11b, 11g, and 802.11n 1T1R
- Short Guard Interval
- Greenfield mode
- STBC in RX mode
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle no-idealities effects from CMOS RF block

1.4 SYSTEM

- Andes Technology N10 processor w/ ILM/DLM and I-cache
- 128K ROM and 192 KB SRAM for Instruction and data SRAM in total
- 8K retention SRAM
- Suspend/Wake-up manger controller
- One UART_Debug

1.5 HOST INTERFACE

- SPI slave
  - Provide proprietary/user CMD
- SDIO , SDIO 2.0 support both 1.8v and 3.3v in VIO
- USB

1.6 SYSTEM CLOCKING AND RESET

The SV615XP has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

1.7 DESIGN FOR TEST

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2 Power Supplies and Power Management

2.1 General Description and PMU Power Connection

The power management unit (PMU) contains Low Dropout Regulators (LDOs), buck DC-DC converter and reference bandgap circuit.

The PMU integrated multi-LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line / load regulation, ripple rejection and output noise.

The input voltage of the buck converter is 3.3V. Its output voltage is 1.6V and feeds into the input power of the RF circuit and DLDO which has 1.2V output voltage for all digital circuits.

Figure 2 shows the typical power connection for SV615XP. DLDO and some RF circuits are powered by the buck converter output. The VDDIO is a power input which may be 3.3V from the host side. The connection structure is shown in the figure below.

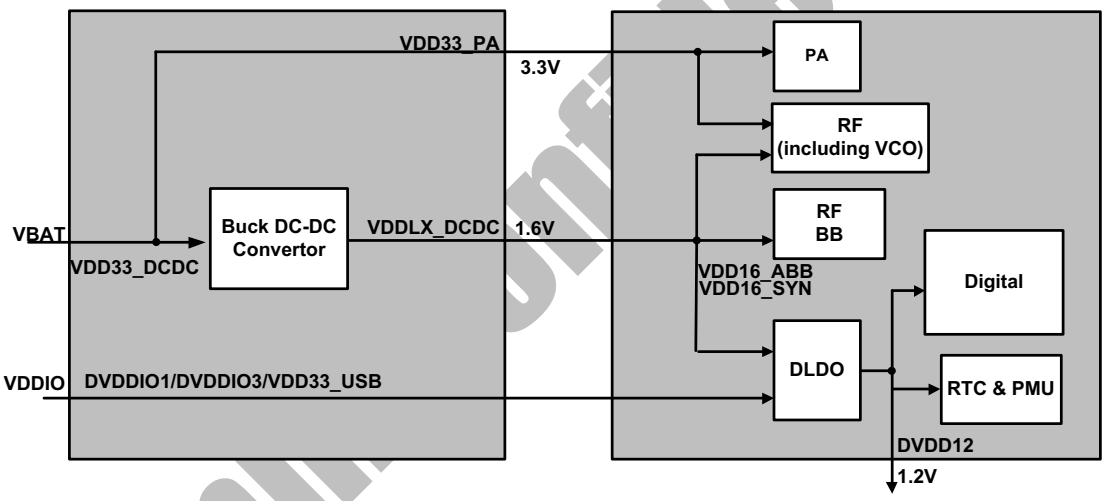


Figure 2: SV615XP Power Connection

2.2 DLDO

The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.6V input to 1.2V output which suits the digital circuits. The input is typically connected to the buck's output.

2.3 Buck Converter

The regulator is a DC-DC step-down converter (buck converter) to source 300mA (max.) with 2.0V to 1.5V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

2.4 Power Management Control

There are three power modes that SV615XP operates when it is initialized: HOST_OFF, ACTIVE mode and SLEEP mode. There are two intermediate system transition modes: FW_DOWNLOAD and WARM_UP mode. The following are the brief introduction to each mode.

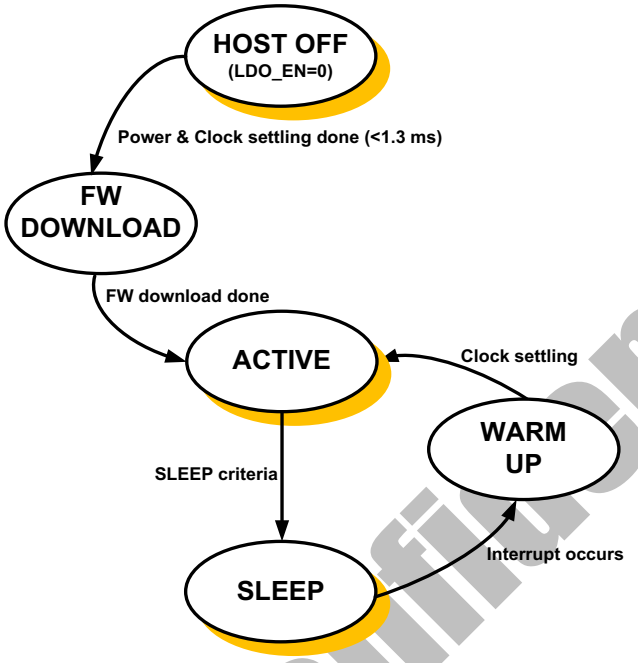


Figure 3: SV615XP Power State

Table 1: SV615XP Power State Description

State	Description
HOST OFF	When **LDO_EN** pin is de-asserted and logically low, the chip is brought to this state immediately.
	Sleep clock and internal power supply is disabled.
	After **LDO_EN** pin is asserted, the internal power and clock will be settled down within 1.3 ms.
FW DOWNLOAD	States for firmware download after power and clock is settled down.
SLEEP	The host controller can determine when to enter sleep to turn off most circuit in SV615XP. All the RF, DPLL circuits are turned off. In sleep mode, the system could be awakened after the sleep time is expired or by an external wake up signal from the host controller.
	All internal states are maintained and the Crystal oscillator is disabled.
WARM UP	The system transitions from SLEEP to ACTIVE. The crystal or oscillator is brought up and the PLL is enabled.
ACTIVE	The high speed clock is operational and sent to each block by the clock control register.
	The RF circuit is enabled to transmit or receive data, and the whole system is under normal operation.

2.5 POWER-ON SEQUENCE

Figure 4 shows the power-on sequence of the SV615XP from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the SV615XP or pulsed low to induce a subsequent reset. After LDO_EN is assert and host starts the power-on sequence of the SV615XP. From that point, the typical SV615XP power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

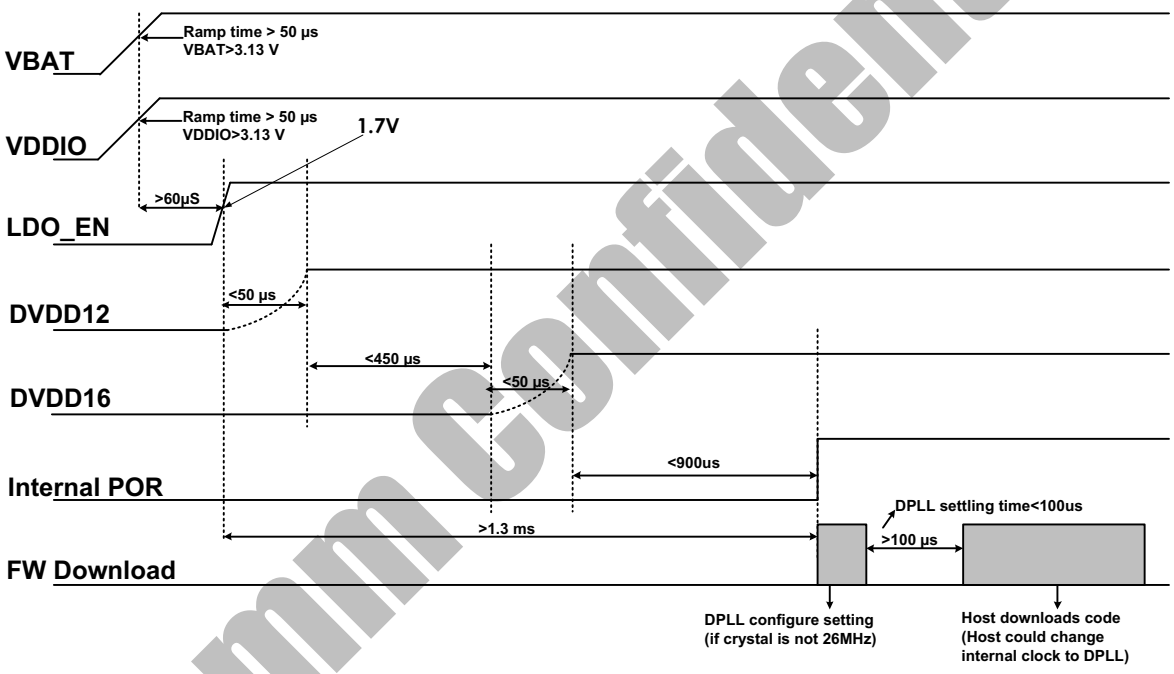


Figure 4 : Power-on sequence

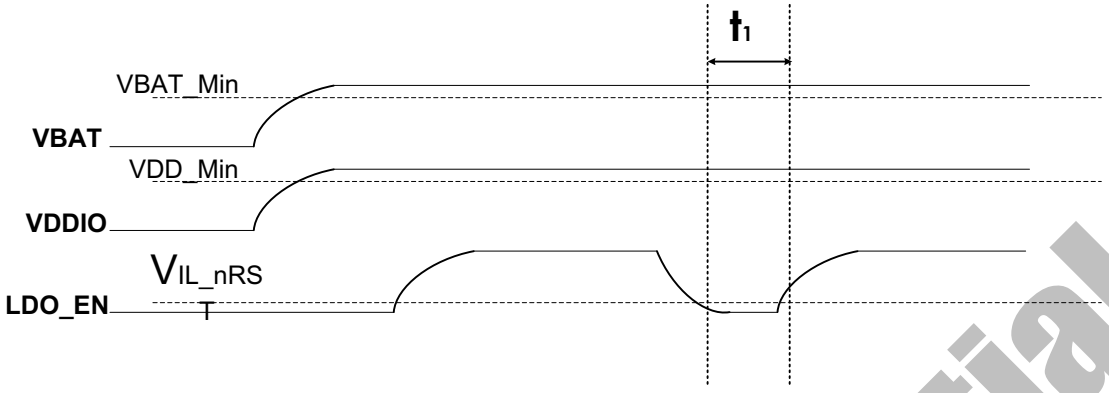


Figure 5 : Reset Timing

Table 2 : Reset Timing Parameters

Parameters	Description	Min.	Unit
t_1	Duration of LDO_EN signal level < V_{IL}_nRST to reset the chip	30	us

2.6 RESET CONTROL

The SV615XP **LDO_EN** pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV615XP is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV615XP turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

3 INTERFACE DESCRIPTION

3.1 SPI TIMING WAVEFORM

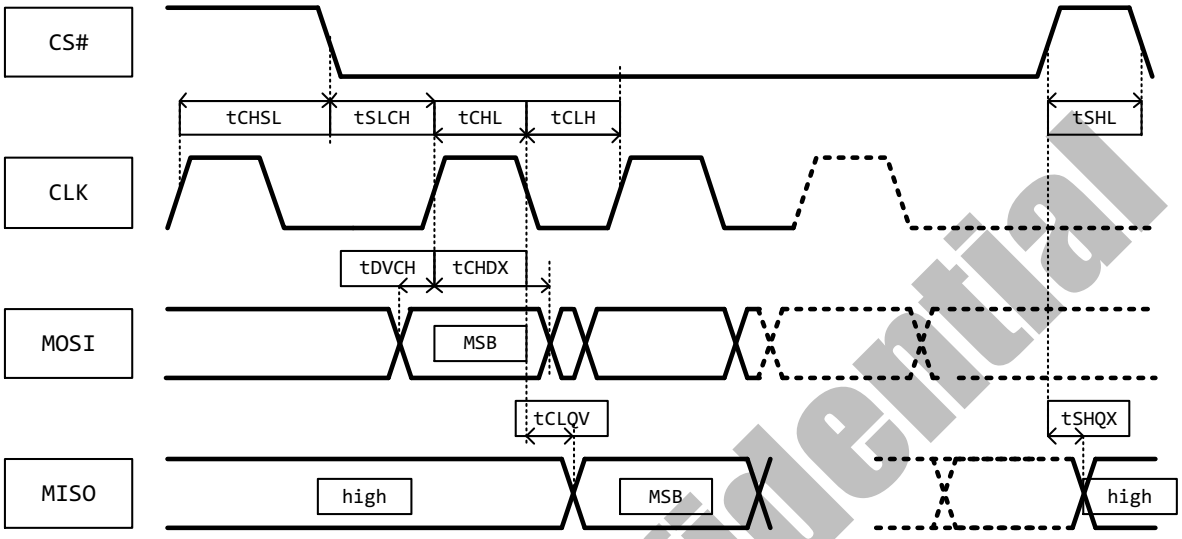


Figure 6 : SPI Timing Waveform

Table 3 : SV6152P SPI Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
tCHSL	CS# active hold time	10			ns
tSLCH	CS# active setup time	3			ns
tSHL	CS# inactive time	300			ns
tCHL	CLK high time	12.5			ns
tCLH	CLK low time	12.5			ns
tDVCH	Data in (MISO) setup time	3			ns
tCHDX	Data in (MISO) hold time	3			ns
tCLQV	Data output delay			6.5	ns
tSHQX	Data output disable time			6	ns

3.2 SDIO TIMING WAVEFORM

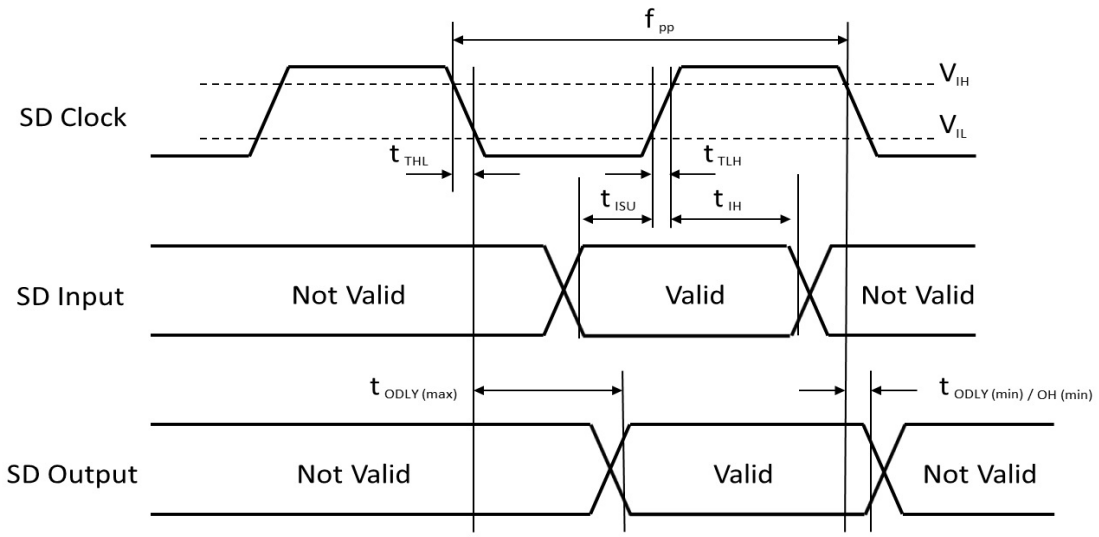


Figure 7 : SDIO TIMING WAVEFORM

Table 4 : SV6152P SDIO version 2.0 Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock CLK (All values are referred to min(V_{IH}) and max (V_{IL}).					
f_{pp}	Clock frequency Data Transfer Mode	0		50	MHz
t_{TLH}	Clock rise time			3	ns
t_{THL}	Clock fall time			3	ns
Inputs CMD, DAT (reference to CLK)					
t_{ISU}	Input set-up time	6			ns
t_{IH}	Input hold time	2			ns
Outputs CMD, DAT (reference to CLK)					
t_{ODLY}	Output Delay time during Data Transfer Mode			14	ns
t_{OH}	Output Hold time	2.5			Ns

3.3 USB Timing Waveform

Table 5: SV6155P USB High-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tHSRLEW	Slew rate of rising edge	-	-	-	1600	V/usec
tHSFLEW	Slew rate of falling edge	-	-	-	1600	V/usec
Driver waveform	-	Specified by eye pattern template in USB2.0 spec.	-	-	-	-
Clock Timings						
THSRDRATE	High-speed data rate		479.76	-	480.24	Mbps
High-Speed Data Timings						
TJ	Data source jitter	Source and receiver jitter specified by the eye pattern template defined in USB2.0 spec.				
RXJT	Receiver jitter tolerance					

Table 6 : SV6155P USB Full-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tFR	Rise time	CL = 50 pF 10% ~ 90% of |VOH – VOL|	4	-	20	ns
tHSFLEW	Fall time	CL = 50 pF 90% ~ 10% of |VOH – VOL|	4	-	20	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	90	-	110	%
Clock Timings						
TFSTXDRATE	Full-speed TX data rate		11.994	-	12.006	Mbps
TFSRXDRATE	Full-speed RX data rate		11.97	-	12.03	Mbps
Full-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-2	-	5	ns
TJR1	Receiver jitter	To next transition	18.5	-	18.5	ns
TJR2	Receiver jitter	For paired transition	-9	-	9	ns
TFEOPT	Source SE0 interval of EOP	-	160	-	175	ns
TFEOPR	Receiver SE0 interval of EOP	-	82	-	-	ns
TFST	Width of SE0 interval during differential transition	-	-	-	14	ns

Table 7: SV6155P USB Low-Speed Source Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						
tFR	Rise time	CL = 200 pF~ 600pF 10% ~ 90% of |VOH–VOL|	75	-	300	ns
tHSFLEW	Fall time	CL = 200pF ~ 600pF 90% ~ 10% of |VOH–VOL|	75	-	300	ns
tFRMA	Differential rise/fall time matching (tFR/tFF)	Specified by eye pattern template in USB2.0 spec.	80	-	125	%
Clock Timings						
TFSTXDRATE	Low-speed TX data rate		1.49925	-	1.50075	Mbps
TFSRXDRATE	Low-speed RX data rate		1.49925	-	1.50075	Mbps
Full-Speed Data Timings						
TFDEOP	Source jitter for differential transition to SE0 transition	-	-40	-	100	ns
TJR1	Receiver jitter	To next transition	-75	-	75	ns
TJR2	Receiver jitter	For paired transition	-45	-	45	ns
TFEOPT	Source SE0 interval of EOP	-	1.25	-	1.5	ns
TFEOPR	Receiver SE0 interval of EOP	-	670	-	-	ns
TFST	Width of SE0 interval during differential transition	-	-	-	210	ns

4 DC CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings in Table 8 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 8: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
VDD16	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD33_SX	VDD input for external components I/O control	-0.3 to 3.6	V
VDD33_RF	VDD input for external components I/O control	-0.3 to 3.6	V
DVDDIO1	VDD input for I/O	-0.3 to 3.6	V
DVDDIO3	VDD input for I/O	-0.3 to 3.6	V
VDD33_USB	VDD input for I/O	-0.3 to 3.6	V
DVDD12	VDD output for internal digital circuit	-0.3 to 1.32	V
VDD16_DCDC	VDD input for digital circuit's LDO	-0.3 to 3.6	V
VDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V

4.2 ENVIRONMENTAL RATINGS

The environmental ratings are shown in Table 9 : Environmental Ratings

Table 9 : Environmental Ratings

	Part Number	Value	Units
Operating Temperature(T_A)	SV6155P	-40 to +85	°C
	SV6152P	-40 to +85	

4.2.1 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

a) Mounted within 168 hours of factory conditions < 30 **°C** /60%RH

b) Storage humidity needs to maintained at <10% RH

c) Baking is necessary if customer exposes the component to air over 168 hours, baking condition: 125°C / 8 hours

4.3 THERMAL CHARACTERISTICS

Thermal characteristics without external heat sink in still air condition

Table 10: The thermal characteristics of the SV615XP

Symbol	Description	Typ.	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance θ_{JA} (°C /W) for JEDEC 4L system PCB	37.8	°C/W
θ_{JC}	Thermal Resistance θ_{JC} (°C /W) for JEDEC 4L system PCB	TBD	°C/W
Ψ_{Jt}	Thermal Characterization parameter Ψ_{Jt} (°C /W) for JEDEC 4L system PCB	4.13	°C/W
	Maximum Lead Temperature (Soldering 10s)	260	°C

Notes: * JEDEC 51-7 system FR4 PCB size: 3" x 4.5" (76.2 x 114.3 mm)
* Thermal characteristics without external heat sink in still air condition

4.4 ELECTROSTATIC DISCHARGE SPECIFICATIONS

This is an ESD sensitive product. Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Table 11: ESD Specifications

Pin Type	Test Condition	ESD Rating	Unit
Human Body Mode (HBM)	refers to MIL-STD-883G Method 3015.7	Pass ±2.5	KV
Charged Device Model(CDM)	JEDEC –500 +500 V specification JESD22-C101, all pins	Pass ±500	V

4.5 POWER-ON HOURS(POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under iComm's standard terms and conditions for iComm semiconductor products.

Table 12: Power-On Hours

OPERATION CONDITION	Part Number	Power-On Hours(POH)(hours)
T_A up to 85°C [a]	SV6155P	87600
T_A up to 85°C [a]	SV6152P	

a. The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

4.6 Recommended Operating Conditions and DC Characteristics

Table 13: Recommended Operating Conditions and DC Characteristics

Domain(Symbol)	Description	Min.	Typ.	Max.	Unit
VDD16	VDD input for analog 1.6V		1.6		V
VDD33_SX	VDD input for external components I/O control	3.13	3.3	3.46	V
VDD33_RF	VDD input for external components I/O control	3.13	3.3	3.46	V
DVDDIO1	VDD input for GPIO pins	3.13	3.3	3.46	V
DVDDIO3	VDD input for GPIO pins (same level as DVDDIO1)	3.13	3.3	3.46	V
VDD33_USB	VDD input for HSDP/HSDM	3.13	3.3	3.46	V
	VDD input for GPIO pins	1.71	3.3	3.46	
DVDD12	VDD output for internal digital circuit		1.2		V
VDD16_DCDC	VDD input for digital circuit's LDO		1.6		V
VDD33_DCDC	VDD input for DCDC	3.13	3.3	3.46	V
(V_{IL})	Input Low voltage when VDDIO=3.3V	-0.3		0.8	V
	Input Low voltage when VDDIO=1.8V	-0.3		0.6	V
(V_{IH})	Input High voltage when VDDIO=3.3V	2		3.6	V
	Input High voltage when VDDIO=1.8V	1.2		3.6	V
(V_{T+})	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.6	1.74	1.89	V
	Schmitt trigger low to high threshold voltage when VDDIO=1.8V	1.03	1.07	1.15	V
(V_{T-})	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.27	1.4	1.56	V
	Schmitt trigger high to low threshold voltage when VDDIO=1.8V	0.67	0.7	0.72	V
(V_{OL})	Output low voltage when VDDIO=3.3V			0.4	V
	Output low voltage when VDDIO=1.8V			0.45	V
(V_{OH})	Output high voltage when VDDIO=3.3V	2.4			V
	Output high voltage when VDDIO=1.8V	1.3			V

Domain (Symbol)	Description	Min.	Typ.	Max.	Unit
(R_{PD})	Input weakly pull-down resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull- down option except that GPIO_5 has internal weakly pull-up option				KΩ
(R_{PU})	Input weakly pull-high resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull- down option except that GPIO_5 has internal weakly pull-up option				KΩ
(I_{OL})	Low level output current @ V_{OL}(max), 8mA setting	11.9	17.7	23.4	mA
	Low level output current @ V_{OL}(max), 12mA setting	15.8	23.5	31.1	mA
(I_{OH})	High level output current @ V_{OH}(min), 8mA setting	17.2	34.1	58.8	mA
	High level output current @ V_{OH}(min), 12mA setting	23.9	47.2	81.5	mA

5 FREQUENCY REFERENCES

5.1 CRYSTAL OSCILLATOR SPECIFICATIONS

Table 14: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
Crystal load Capacitance	–	–	10		pF
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm

5.2 EXTERNAL CLOCK-REQUIREMENTS AND PERFORMANCE

Table 15: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
OSCIN Input Voltage	AC-couple analog signal	400	–	1500	mV_{PP}
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm
Duty Cycle	26MHz clock	40	50	60	%
Phase Noise (802.11b/g)	26MHz clock at 1KHz offset	–	–	–119	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–129	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–134	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–139	dBc/Hz
Phase Noise (802.11n 2.4)	26MHz clock at 1KHz offset	–	–	–125	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–135	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–140	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–145	dBc/Hz

6 Electrical Specifications

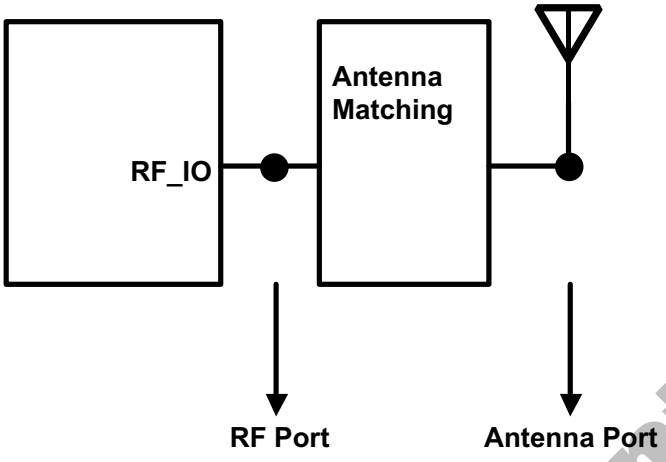


Figure 8: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the RF Port unless otherwise specified.

6.1 LAN RF PERFORMANCE SPECIFICATIONS

Table 16: 2.4G WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-95.5		dBm
	CCK, 2 Mbps		-93.5		dBm
	CCK, 5.5 Mbps		-91.0		dBm
	CCK, 11 Mbps		-88.0		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.5		dBm
	OFDM, 9 Mbps		-90.0		dBm
	OFDM, 12 Mbps		-88.0		dBm
	OFDM, 18 Mbps		-86.0		dBm
	OFDM, 24 Mbps		-82.5		dBm
	OFDM, 36 Mbps		-79.5		dBm
	OFDM, 48 Mbps		-74.5		dBm
	OFDM, 54 Mbps		-73.5		dBm
Rx Sensitivity (HT20) Greenfield 800nS GI Non-STBC	HT20, MCS0		-91.0		dBm
	HT20, MCS1		-88.0		dBm
	HT20, MCS2		-86.0		dBm
	HT20, MCS3		-81.5		dBm
	HT20, MCS4		-79.0		dBm
	HT20, MCS5		-74.5		dBm
	HT20, MCS6		-73.5		dBm
	HT20, MCS7		-72.5		dBm
Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
RX Adjacent Channel Rejection (CCK)	CCK, 1 Mbps (30 MHz offset)		41		dB
	CCK, 11 Mbps (25 MHz offset)		41		dB
RX Adjacent Channel Rejection (OFDM)	OFDM, 6 Mbps (25 MHz offset)		39		dB
	OFDM, 54 Mbps (25 MHz offset)		23		dB
RX Adjacent Channel Rejection (HT20)	HT20, MCS0 (25 MHz offset)		38		dB
	HT20, MCS7 (25 MHz offset)		21		dB
TX Output Power (with PADPD)	CCK, 1-11 Mbps		19		dBm
	OFDM, 54 Mbps		16		dBm
	HT20, MCS7		15		dBm

7 System Power Consumption

Table 17: Power Consumption at DCDC mode (DCDC buck convertor is enable)

WLAN Operational Modes	Typ.[d]	Unit
OFF[a]	2	uA
Rx, CCK, 1 Mbps	68	mA
Rx, OFDM, 54 Mbps	68	mA
Rx, HT20, MCS7	68	mA
Rx, HT40, MCS7	75	mA
Tx, CCK, 1 Mbps	307	mA
Tx, OFDM, 54 Mbps@15dBm	256	mA
Tx, HT20, MCS7@15dBm	260	mA
Tx, HT40, MCS7@15dBm	260	mA

Table 18: Power Consumption at LDO mode (DCDC buck convertor is disable)

WLAN Operational Modes	Typ.[d]	Unit
OFF[a]	2	uA
Rx, CCK, 1 Mbps	113	mA
Rx, OFDM, 54 Mbps	113	mA
Rx, HT20, MCS7	113	mA
Rx, HT40, MCS7	124	mA
Tx, CCK, 1 Mbps@18dBm	328	mA
Tx, OFDM, 54 Mbps@15dBm	280	mA
Tx, HT20, MCS7@15dBm	283	mA
Tx, HT40, MCS7@15dBm	285	mA

a. OFF mode test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V.
b. Intra-beacon Sleep when MCU is turn on.
   It is used in the applications that require the CPU to be working.
c. Intra-beacon Sleep when MCU is turn off.
d. Conditions: VBAT at 3.3v, VDDIO at 3.3V, 25°C.

8 Pin Descriptions

This section contains a listing of the signal descriptions (see Figure 9/Figure 10 for the SV615XP QFN package pin-out)

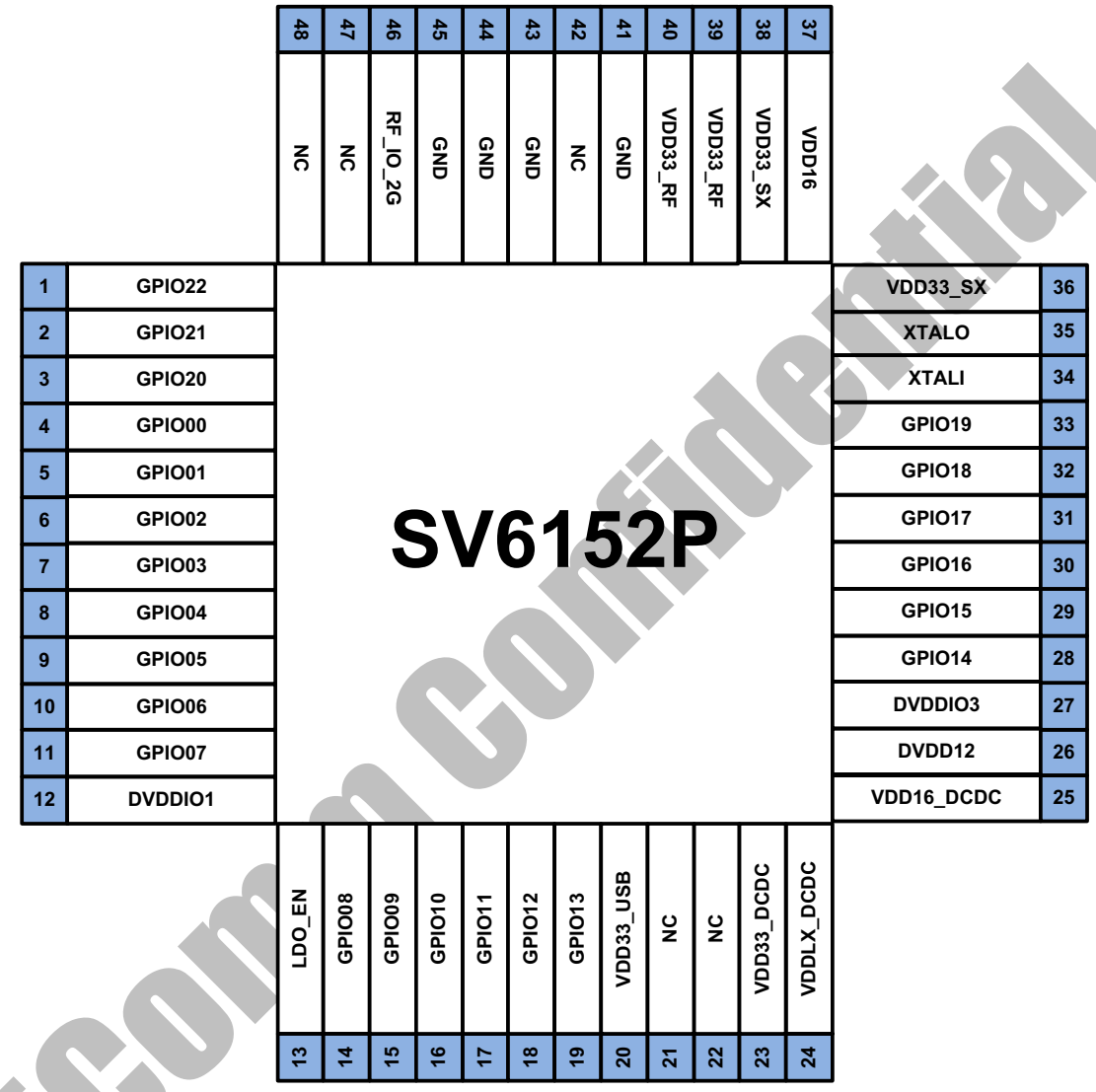


Figure 9: SV6152P QFN Pin Assignment (top view)

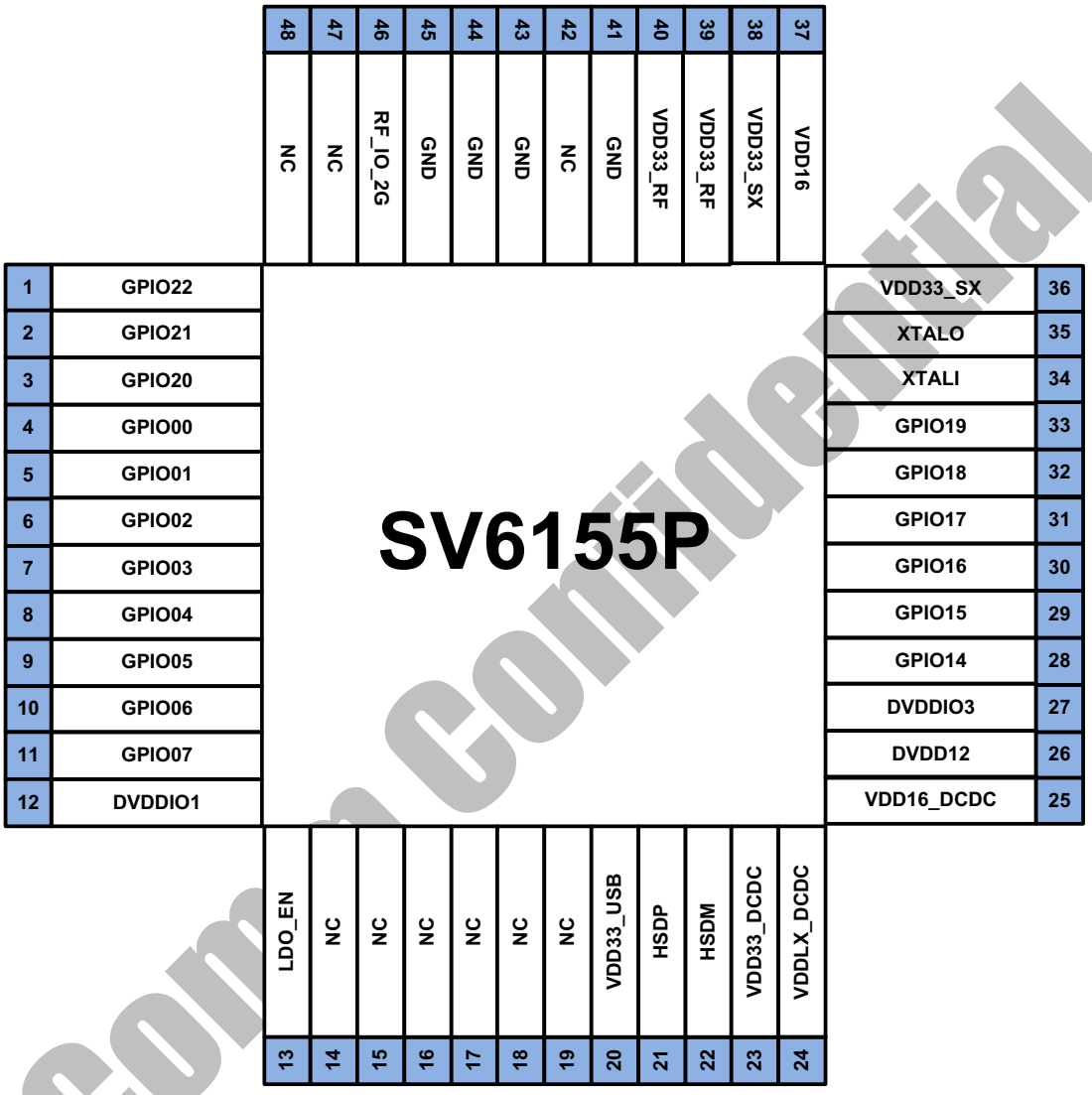


Figure 10: SV6155P QFN Pin Assignment (top view)

Table 19: SV615XP Package Pin-out

No.	Name	Description	Type (default)
1	GPIO22	General Purpose I/O Pins	I/O
2	GPIO21	General Purpose I/O Pins	I/O
3	GPIO20	Strapping Purpose I/O Pins	I/O
4	GPIO00	General Purpose I/O Pins	I/O
5	GPIO01	General Purpose I/O Pins	I/O
6	GPIO02	General Purpose I/O Pins	I/O
7	GPIO03	General Purpose I/O Pins	I/O
8	GPIO04	General Purpose I/O Pins	I/O
9	GPIO05	General Purpose I/O Pins	I/O
10	GPIO06	General Purpose I/O Pins	I/O
11	GPIO07	Strapping Purpose I/O Pins	I/O
12	DVDDIO1	VIO input for GPIO00~07/GPIO20~22	Power
13	LDO_EN	Reset signal to power down IC	Input
14	GPIO08	General Purpose I/O Pins (NC pin @ SV6155P)	I/O
15	GPIO09	General Purpose I/O Pins (NC pin @ SV6155P)	I/O
16	GPIO10	General Purpose I/O Pins (NC pin @ SV6155P)	I/O
17	GPIO11	General Purpose I/O Pins (NC pin @ SV6155P)	I/O
18	GPIO12	General Purpose I/O Pins (NC pin @ SV6155P)	I/O
19	GPIO13	General Purpose I/O Pins (NC pin @ SV6155P)	I/O
20	VDD33_USB	VIO input for GPIO08~13/HSDP/HSDM	Power
21	HSDP	HSDP (NC pin @ SV6152P)	I/O
22	HSDM	HSDM (NC pin @ SV6152P)	I/O
23	VDD33_DCDC	analog 3.3V input for DCDC	Power
24	VDDLX_DCDC	DCDC buck regulator: output to inductor	Power
25	VDD16_DCDC	DCDC 1.6V	Power
26	DVDD12	Digital 1.2V input	Power
27	DVDDIO3	VIO input for GPIO14~19	Power
28	GPIO14	Strapping Purpose I/O Pins	I/O
29	GPIO15	Strapping Purpose I/O Pins	I/O
30	GPIO16	General Purpose I/O Pins	I/O
31	GPIO17	General Purpose I/O Pins	I/O
32	GPIO18	General Purpose I/O Pins	I/O
33	GPIO19	General Purpose I/O Pins	I/O
34	XTALI	Input of crystal clock reference	Input
35	XTALO	Output of crystal clock reference	Output
36	VDD33_SX	analog 3.3V input	Power
37	VDD16	analog 1.6V input	Power
38	VDD33_SX	analog 3.3V input	Power
39	VDD33_RF	analog 3.3V input	Power
40	VDD33_RF	analog 3.3V input	Power
41	GND	Ground	GND
42	NC	NC Pin	NC
43	GND	Ground	GND

No.	Name	Description	Type (default)
44	GND	Ground	GND
45	GND	Ground	GND
46	RF_IO_2G	2.4 GHz RF input & output port	RF I/O
47	NC	NC Pin	NC
48	NC	NC Pin	NC

8.1 Interface Selection

SV615XP has bootstrap pins to select interface which including debug interface, host I/O. There are GPIO07, GPIO14, GPIO15 and GPIO20 (see Table 20 for detail). The bootstrap pin of GPIO07 decides switching the debug interface out to GPIOs (see Table 21 for detail). The bootstrap pins of GPIO14 and GPIO15 decode switch the host IO (SPI DATA slave/SDIO/USB) out to GPIOs (see Table 22/Table 23/Table 24 for detail). The bootstrap pin of GPIO20 decides switching 25MHz or 40MHz clock when using USB interface.

Table 20: The strapping truth table

strapping truth table		
	Interface mode	**Description**
GPIO[07]		
0	ICE debug	for ICE debug interface
1	NC	NC (default)
GPIO[15], GPIO[14]		
01	SPIDATA	SPI data mode
10	SDIO	SDIO mode
11	USB	USB mode
GPIO[20]		
0	USB_XO25M	for USB 25MHz clock (default)
1	USB_XO40M	for USB 40MHz clock

Table 21: The strapping pin of GPIO07

GPIO07		Low			High		
Pin No.	**Name**	**I/O**	**PULL**	**I/O Function**	**I/O**	**PULL**	**I/O Function**
4	**GPIO00**	I/O	F	TMSC	I/O	F	NC
5	**GPIO01**	I	F	TCKC	I	F	NC
6	**GPIO02**	I	PU	nSRST	I	PU	NC
7	**GPIO03**	I	F	UART0_RXD	I	F	NC
8	**GPIO04**	O	F	UART0_TXD	O	F	NC

Table 22 : The strapping pin of GPIO14/15 for SPI DATA slave interface

GPIO15/14		2'b01		
Pin No.	Name	I/O	PULL	I/O Function
9	GPIO05	O	F	NC
10	GPIO06	I	F	NC
11	GPIO07	O	PU	Strapping
14	GPIO08	O	F	SPI0_S_INT
15	GPIO09	I	F	NC
16	GPIO10	I	F	SPI0_S_MOSI
17	GPIO11	I	F	SPI0_S_CLK
18	GPIO12	O	F	SPI0_S_MISO
19	GPIO13	I	F	SPI0_S_CSN
28	GPIO14	I/O	F	Strapping
29	GPIO15	I/O	F	Strapping
30	GPIO16	I/O	F	NC
31	GPIO17	I/O	F	NC
32	GPIO18	I/O	F	NC
33	GPIO19	I/O	F	NC
3	GPIO20	O	F	GPIO20(WIFI_WAKE_HOST)
2	GPIO21	I	F	GPIO21(HOST_WAKE_WIFI)
1	GPIO22	O	F	NC

Table 23: The strapping pin of GPIO14/15 for SDIO interface

GPIO15/14		2'b10		
Pin No.	Name	I/O	PULL	I/O Function
9	GPIO05	O	F	NC
10	GPIO06	I	F	NC
11	GPIO07	O	PU	Strapping
14	GPIO08	I/O	F	SD_D2
15	GPIO09	I	F	SD_D3
16	GPIO10	I/O	F	SD_CMD
17	GPIO11	I/O	F	SD_CLK
18	GPIO12	I/O	F	SD_D0
19	GPIO13	O	F	SD_D1
28	GPIO14	I/O	F	Strapping
29	GPIO15	O	F	Strapping
30	GPIO16	I/O	F	NC
31	GPIO17	O	F	NC
32	GPIO18	I/O	F	NC
33	GPIO19	I/O	F	NC
3	GPIO20	I/O	F	GPIO20(WIFI_WAKE_HOST)
2	GPIO21	I	F	GPIO21(HOST_WAKE_WIFI)
1	GPIO22	I/O	F	NC

Table 24: The strapping pin of GPIO14/15 for USB slave interface

GPIO15/14		2'b11		
Pin No.	**Name**	**I/O**	**PULL**	**I/O Function**
9	**GPIO05**	O	F	NC
10	**GPIO06**	I	F	NC
11	**GPIO07**	O	PU	Strapping
14	**GPIO08**	O	F	NC
15	**GPIO09**	I	F	NC
16	**GPIO10**	I	F	NC
17	**GPIO11**	I	F	NC
18	**GPIO12**	O	F	NC
19	**GPIO13**	I	F	NC
28	**GPIO14**	I/O	F	Strapping
29	**GPIO15**	I/O	F	Strapping
30	**GPIO16**	I/O	F	NC
31	**GPIO17**	I/O	F	NC
32	**GPIO18**	I/O	F	NC
33	**GPIO19**	I/O	F	NC
3	**GPIO20**	O	F	GPIO20(WIFI_WAKE_HOST)
2	**GPIO21**	I	F	GPIO21(HOST_WAKE_WIFI)
1	**GPIO22**	O	F	NC

8.2 User Define I/O Function Selection

After bootstrap, the SV615XP also provides a pad multiplex switching from the bootstrap function to selected I/O function by register signals. There is a condition to leave bootstrap function. That is switching to GPIO first then switching to select I/O function. The Table 25 shows the all I/O functions for each PAD.

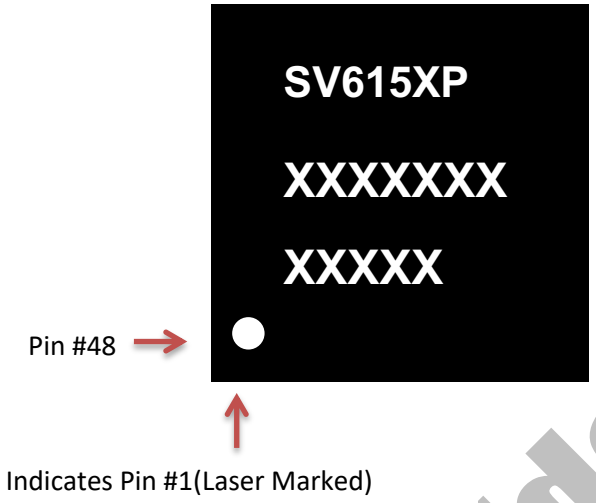
Table 25: The PAD multiplex for each PAD

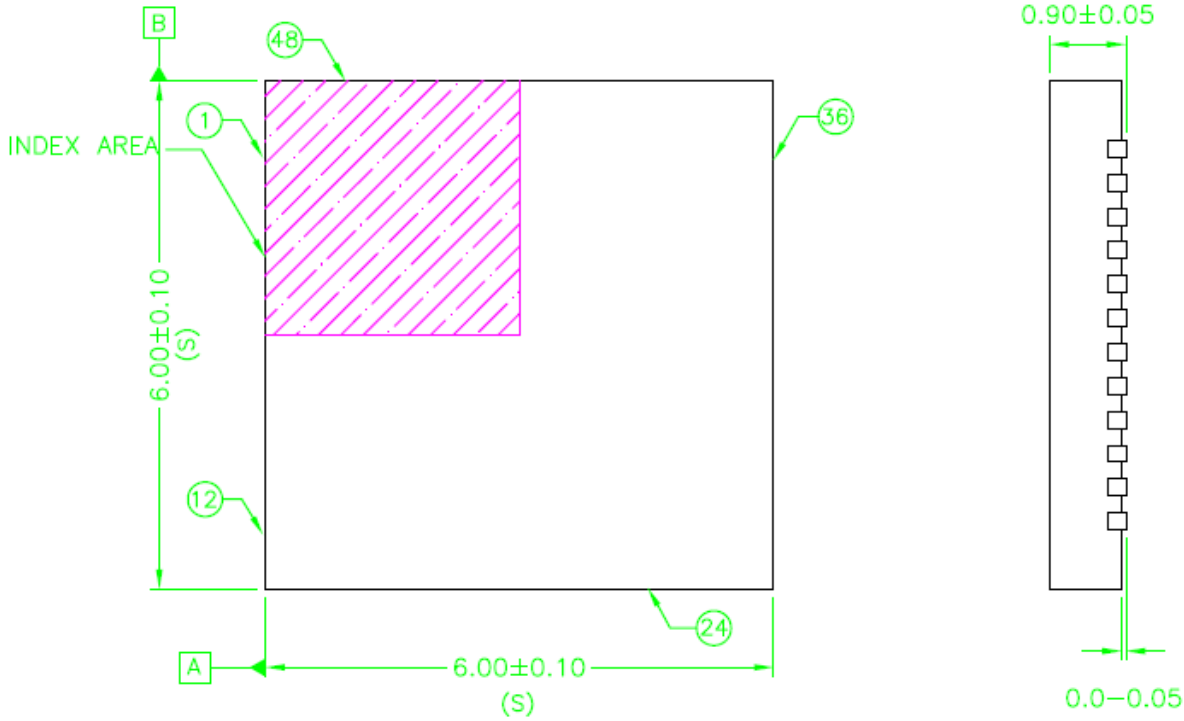
Pin No.	Pin Name	Alternate Functions		
4	GPIO00	I/O	F	GPIO[00]
5	GPIO01	I/O	F	GPIO[01]
6	GPIO02	I/O	F	GPIO[02]
7	GPIO03	I/O	F	GPIO[03]
8	GPIO04	I/O	F	GPIO[04]
9	GPIO05	I/O	F	GPIO[05]
10	GPIO06	I/O	F	GPIO[06]
11	GPIO07	I/O	F	GPIO[07]
14	GPIO08	I/O	F	GPIO[08]
15	GPIO09	I/O	F	GPIO[09]
16	GPIO10	I/O	F	GPIO[10]
17	GPIO11	I/O	F	GPIO[11]
18	GPIO12	I/O	F	GPIO[12]
19	GPIO13	I/O	F	GPIO[13]
28	GPIO14	I/O	F	GPIO[14]
29	GPIO15	I/O	F	GPIO[15]
30	GPIO16	I/O	F	GPIO[16]
31	GPIO17	I/O	F	GPIO[17]
32	GPIO18	I/O	F	GPIO[18]
33	GPIO19	I/O	F	GPIO[19]
3	GPIO20	I/O	F	GPIO[20]
2	GPIO21	I/O	F	GPIO[21]
1	GPIO22	I/O	F	GPIO[22]

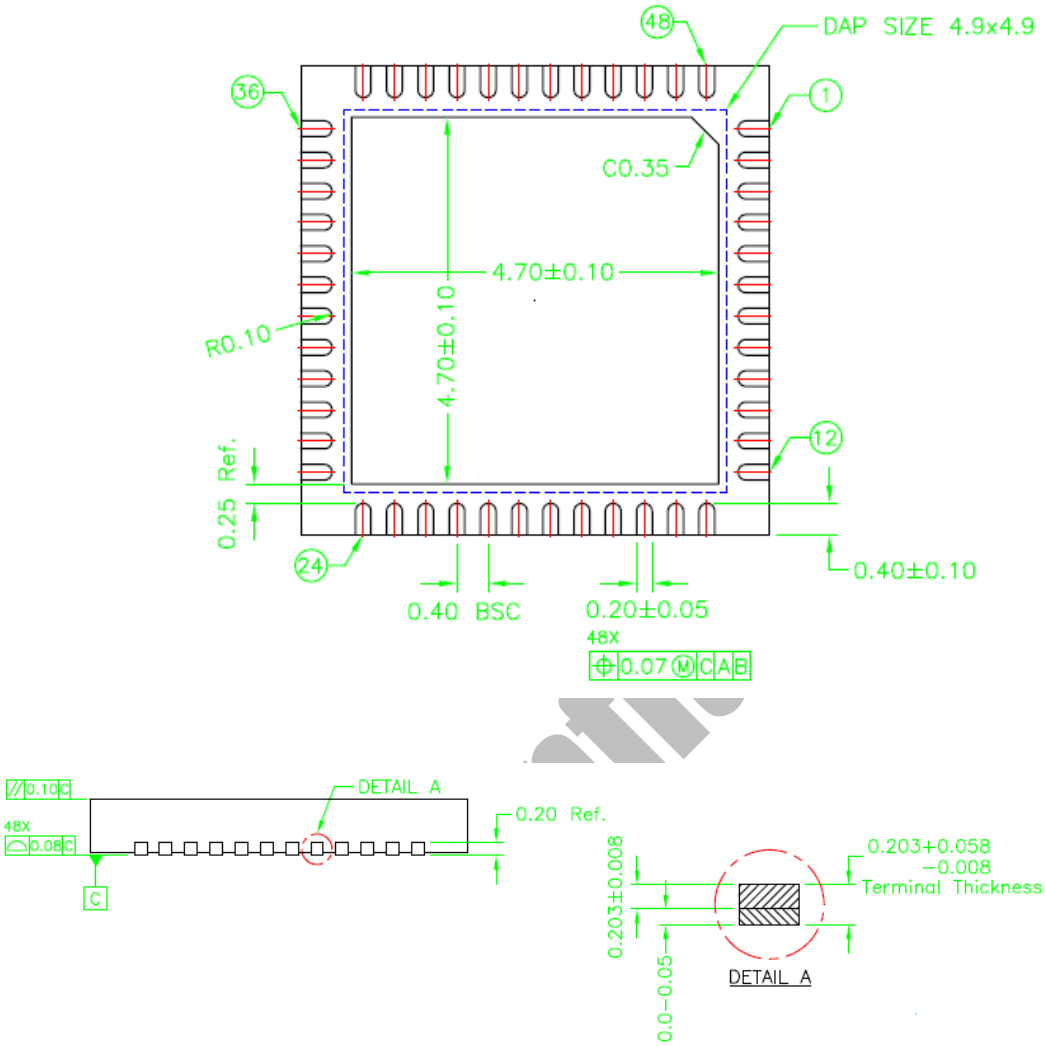
9 PACKAGE INFORMATION

6 x 6 mm (body size), 0.4mm pitch QFN-48

Marking format (top view)







NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. L/F STOCK# FR9012 (PPF)

Figure 11: SV615XP QFN 6 x 6 mm Package Dimensions

10 Part Number

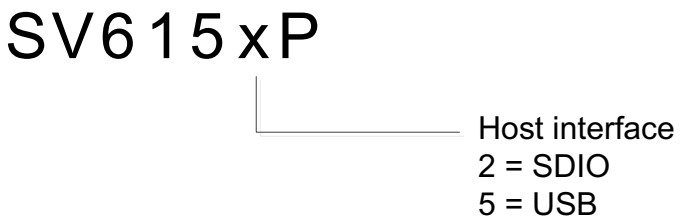


Figure 12: SV615XP Part Number

The table below provides the ordering information of the SV615XP series of chips.

Table 26: SV615XP Part Number

Part number	Band	Embedded Flash or PSRAM or N.A.	Operating Temp (°C)	Package
SV6152P	Single	No embedded	-40 to +85	QFN 6x6
SV6155P	Single	No embedded	-40 to +85	QFN 6x6